**3. VHDL code for full adder using structural modeling**  
  
  
  
**Step1: VHDL code for Half Adder:**  
  
  
  
library IEEE;  
use IEEE.STD\_LOGIC\_1164.ALL;  
entity test\_HA is  
Port ( a : in STD\_LOGIC;  
b : in STD\_LOGIC;  
sum : out STD\_LOGIC;  
cout : out STD\_LOGIC);  
end test\_HA;  
architecture data\_flow\_test of test\_HA is  
begin  
sum<= a xor b;  
cout<= a and b;  
end data\_flow\_test;  
  
  
  
**Step 2: VHDL code for OR gate:**  
  
  
  
library IEEE;  
use IEEE.STD\_LOGIC\_1164.ALL;  
entity test\_or is  
Port ( p : in STD\_LOGIC;  
q : in STD\_LOGIC;  
r : out STD\_LOGIC);  
end test\_or;  
architecture data\_flow\_test of test\_or is  
begin  
r<= p or q;  
end data\_flow\_test;  
  
  
  
**Step3VHDL code for full adder using structural modeling:**  
  
  
  
library IEEE;  
use IEEE.STD\_LOGIC\_1164.ALL;  
entity test\_Full\_Adder is  
Port ( x : in STD\_LOGIC;  
y : in STD\_LOGIC;  
z : in STD\_LOGIC;  
sum : out STD\_LOGIC;cout : out STD\_LOGIC);  
end test\_Full\_Adder;  
architecture Structural\_test of test\_Full\_Adder is  
component test\_HA is  
Port ( a : in STD\_LOGIC;  
b : in STD\_LOGIC;  
sum : out STD\_LOGIC;  
cout : out STD\_LOGIC);  
end component;  
component test\_or is  
Port ( p : in STD\_LOGIC;  
q : in STD\_LOGIC;  
r : out STD\_LOGIC);  
end component;  
signal sum1,carry1,carry2:STD\_LOGIC;  
begin  
comp1:test\_HA port map(x,y,sum1,carry1);  
comp2:test\_HA port map(sum1,z,sum,carry2);  
comp3:test\_or port map(carry1,carry2,cout);  
end Structural\_test;  
  
  
  
**Test bench Code for Full Adder:**  
  
  
  
LIBRARY ieee;  
USE ieee.std\_logic\_1164.ALL;  
ENTITY tb\_test\_fa IS  
END tb\_test\_fa;  
ARCHITECTURE behavior OF tb\_test\_fa IS  
COMPONENT test\_Full\_Adder  
PORT(  
x : IN std\_logic;  
y : IN std\_logic;  
z : IN std\_logic;  
sum : OUT std\_logic;  
cout : OUT std\_logic  
);  
END COMPONENT;  
--Inputs  
signal x : std\_logic := '0';  
signal y : std\_logic := '0';  
signal z : std\_logic := '0';  
--Outputs  
signal sum : std\_logic;  
signal cout : std\_logic;  
-- No clocks detected in port list. Replace <clock> below with  
-- appropriate port name  
BEGIN  
-- Instantiate the Unit Under Test (UUT)  
uut: test\_Full\_Adder PORT MAP (  
x => x,  
y => y,  
z => z,  
sum => sum,  
cout => cout  
);-- Stimulus process  
process  
begin  
x <= '0';  
y <= '0';  
z <= '0';  
wait for 10 ns;  
x <= '0';  
y <= '0';  
z <= '1';  
wait for 10 ns;  
x <= '0';  
y <= '1';  
z <= '0';  
wait for 10 ns;  
x <= '0';  
y <= '1';  
z <= '1';  
wait for 10 ns;  
x <= '1';  
y <= '0';  
z <= '0';  
wait for 10 ns;  
x <= '1';  
y <= '0';  
z <= '1';  
wait for 10 ns;  
x <= '1';  
y <= '1';  
z <= '0';  
wait for 10 ns;  
x <= '1';  
y <= '1';  
z <= '1';  
wait for 10 ns;  
end process;  
END